40V Sync. Four-Switch DC-DC Boost-Buck Converter

Features

- Single inductor boost buck controller for boost/buck DC/DC conversion
- Wide input voltage range: 4.5V to 40V
- High efficiency
- Switching frequency adjustable and programmable
- External soft start
- Automatic recovery after malfunction
- Output line voltage drop compensation function
- Programmable overcurrent setting
- Normal power indication and output overvoltage protection
- Overheat protection
- Heat enhanced QFN4x4-24L package
- Compliant with RoHS standards

Applications

- Car charger
- Rechargeable portable devices
- USB power supply
- Automotive industry

General Description

AD9575 is a synchronous four switch buck boost DC/DC controller that can regulate the output voltage equal to, higher than, or lower than the input voltage.

The AD9575 can operate within a wide input voltage range of 4.5V to 40V to support various applications.AD9575 adopts current mode control in both step-down and step-up modes to achieve excellent load and line regulation. The switching frequency is programmed by an external resistor.

The device also has programmable soft start function and provides protection functions, including cycle by cycle current limitation, input undervoltage lockout (UVLO), output overvoltage protection (OVP), and thermal shutdown.

The AD9575 is packaged in QFN4x4-24L, providing a very compact system solution and good thermal conductivity.

Typical Application

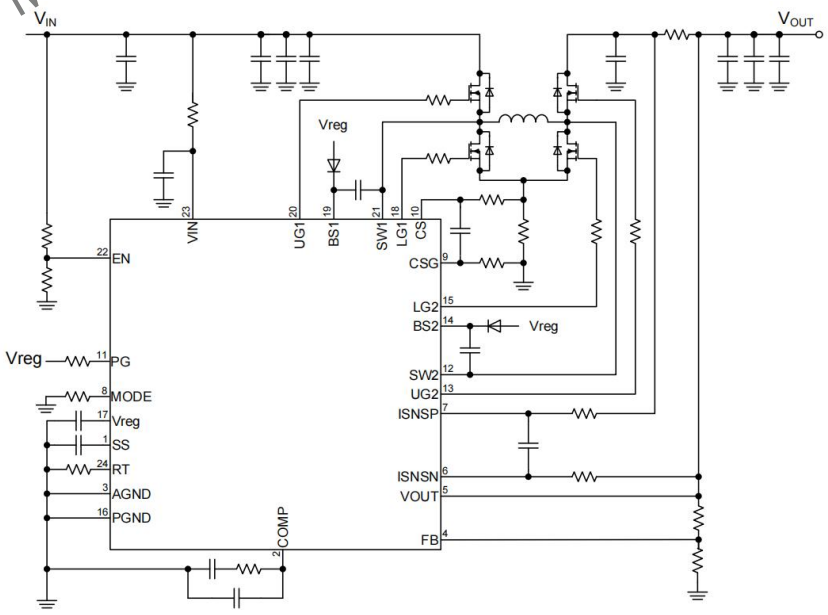
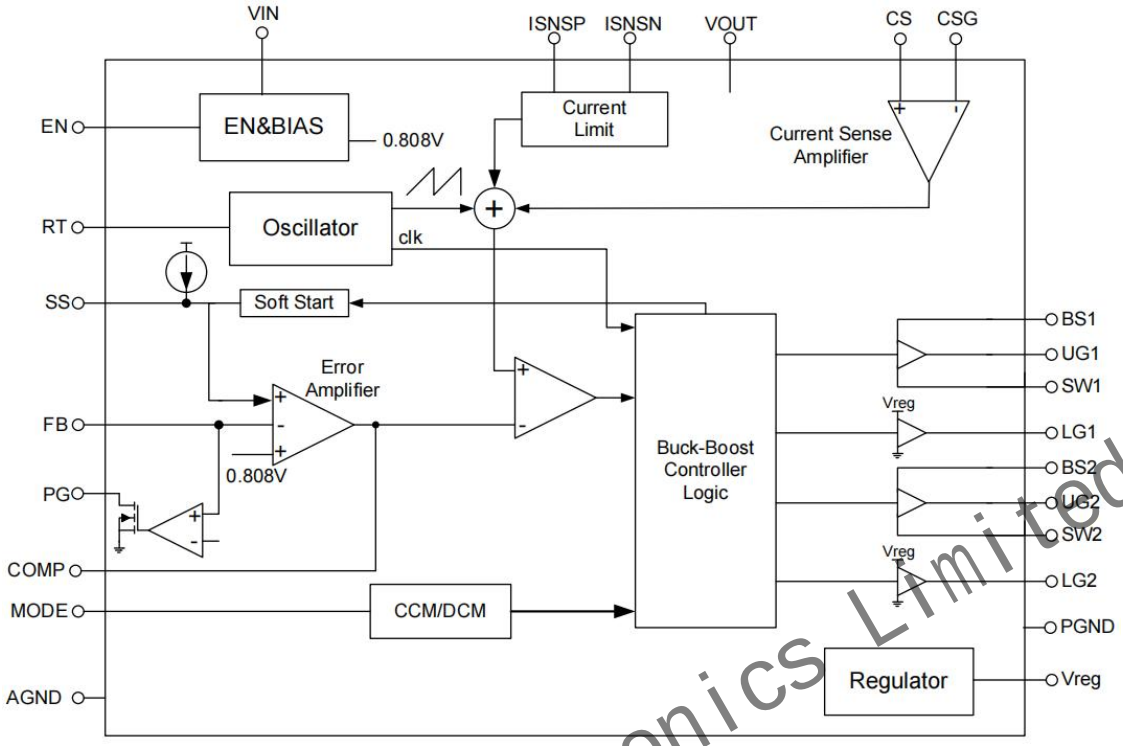


Figure 1. Typical Application Circuit

Block Diagram



Applications Information

AD9575 is a four switch buck boost controller IC that integrates an N-channel MOSFET driver.

When the input voltage (VIN) is higher than the output voltage (VOUT), AD9575 operates in buck mode; When the input voltage is lower than the output voltage, operate in boost mode; When the input voltage approaches the output voltage, it operates in a step-down step-up mode.

The AD9575 integrates four N-channel MOSFET drivers, including two low side drivers and two high side drivers, eliminating the need for additional external drivers or floating bias power supplies. The internal VCC regulator provides power to the internal bias circuit and MOSFET gate driver.

The PWM control scheme adopts valley current mode control (for step-down operation) and peak current mode control (for step-up operation). The inductor current is detected through a single detection resistor connected in series with the low side MOSFET. At the same time, the detection current is also used for monitoring the periodic current limit.

In addition to the cycle by cycle current limiting function, the AD9575 also provides output current regulation function, which can be configured as output current limiting and short-circuit protection. This is very practical for applications that require constant current behavior, such as battery charging.

The soft start time of AD9575 can be programmed to connect to the capacitor of the SS pin to minimize surge current and overshoot during startup. The EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The PG output signal indicates that the system is in good condition when the FB voltage is within the ± 10% adjustment window centered around VREF.

Acontrol loop

ADAD9575 is a fixed frequency current mode controller designed for buck and boost switches. During normal operation, the output voltage is detected at the FB pin through a resistive divider and amplified by an error amplifier. The error amplifier generates an error voltage by driving the COMP pin. The slope compensation signal based on the input voltage (VIN) and output voltage (VOUT) will be added to the current detection signal measured across the CS and CSG pins. The PWM comparator compares this result with the error voltage of the COMP pin.

The AD9575 uses valley current mode control (buck mode) and peak current mode control (boost mode) to regulate the output voltage.

Valley current mode control (buck mode): The high side buck MOSFET (controlled by UG1) is turned on by a PWM comparator at the valley of the inductor ripple current and turned off when the oscillator clock signal arrives. The valley current mode control has advantages for buck converters that need to solve the problem of short conduction time.

Peak current mode control (boost mode): The low side boost MOSFET (controlled by LG2) is turned on by the clock signal in each switching cycle and turned off by the PWM comparator at the peak of the inductor ripple current.

LG1 and UG1 drive signals control the synchronous buck stage, while LG2 and UG2 drive signals control the synchronous boost stage. When VIN approaches VOUT, AD9575 operates using a buck boost transition scheme.

VCC voltage regulator

In AD9575, the VCC regulator provides a regulated 5.4V power supply voltage to the gate driver. When the input voltage (VIN) is low, please ensure that the VCC voltage is sufficient to fully drive the MOSFET. It is recommended to connect a capacitor of 2.2 μ F to 4.7 μ F between VCC and PGND to meet the transient load requirements of the VCC regulator.

Soft start

The soft start time of AD9575 is programmed through the soft start capacitor from the SS pin to AGND. When the converter is enabled, the internal 6 μ A current source will charge the soft start capacitor. When the SS pin voltage is lower than the feedback reference voltage VREF (0.808V), the FB pin voltage is regulated by the soft start pin voltage control. Once the SS voltage exceeds VREF, the soft start phase is completed, and the error amplifier uses VREF as a reference.The approximate formula for soft start time is:

$$t_{ss} = \frac{Css \times 0.808}{6uA}$$

When the converter is disabled due to the EN/UVLO pin being below the operating threshold or VCC being below the VCCUV threshold, the soft start capacitor will be internally discharged. When the converter is in periodic current limiting mode or over temperature protection mode, the soft start pin will also be discharged.

Overcurrent protection function

AAD9575 provides cycle by cycle current limiting function to prevent overcurrent and short circuit situations. In buck mode, the valley voltage detected through CSG and CS pins is limited to 76mV. If the detected voltage does not drop during the off time of the buck switch.

Below this threshold, the high side buck switch skips one switching cycle.

In boost mode, the maximum peak voltage detected through the CS and CSG pins is limited to 170mV. If the peak current of the low side boost switch causes the CS pin voltage to exceed this threshold voltage, the boost switch will be turned off for the remaining time of this clock cycle.

Output current limit

AAD9575 provides output current limiting function and output short circuit protection to limit the output current of DC/DC converters. A current detection amplifier with ISNSP and ISNSN pin inputs monitors the voltage on the shunt resistor and compares it with an internal 50mV reference voltage. The current limiting function can be used in applications that require stable load current.

The constant current of the target can be calculated using the following formula:

$$I_{out,AVG} = \frac{50mV}{Rsns}$$

Shorting the ISNSP and ISNSN pins will disable the current detection function.

Input under-voltage lockout

When AD9575 is powered on, the internal circuit remains inactive until VIN exceeds the input UVLO threshold voltage. When VIN is below the input UVLO threshold voltage, the voltage regulator will be disabled.

Over-temperature protection

The AD9575 integrates an over temperature protection circuit to prevent overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the voltage regulator will shut down.

Layout Guide

The basic PCB layout requires separating sensitive signal paths from power paths. It is recommended to follow the following layout guidelines:

1.The routing of the main current path should be as short and wide as possible to minimize parasitic inductance and resistance.

2.2. Place the input filtering capacitor CIN, step-down power MOSFETs (UG1 and LG1), and detection resistor as close as possible to minimize the loop area of the input switch current in step-down mode.

3. Place the output filtering capacitor COUP, boost power MOSFETs (UG2 and LG2), and detection resistor as close as possible to minimize the loop area of the output switch current in boost mode.

4. Use a combination of large capacity capacitors and small ceramic capacitors with low series impedance for input and output capacitors. Place the small capacitor close to the IC.

5. Minimize the area of the SW1 and SW2 circuits.

6. Place the BST1 startup capacitor close to the IC and directly connect it between the BST1 and SW1 pins.

7. Place the BST2 startup capacitor close to the IC and directly connect it between the BST2 and SW2 pins.

8. Place the feedback resistor near the FB pin. The feedback network is connected after the output capacitor.

9. Place the compensation component near the COMP pin.

10. Arrange sensitive signals (FB, COMP, ISNSP, ISNSN, CS, CSG, Veleg, VOUT, RT, SS) away from switch signals.

11. For the current detection signals CS and CSG, connect them to the detection resistor using Kelvin.

12. For the current detection signals ISNSP and ISNSN, connect them to the detection resistor using Kelvin.

13. Connect all simulated grounds to a common node, and then connect the common node to the power ground behind the output capacitor.

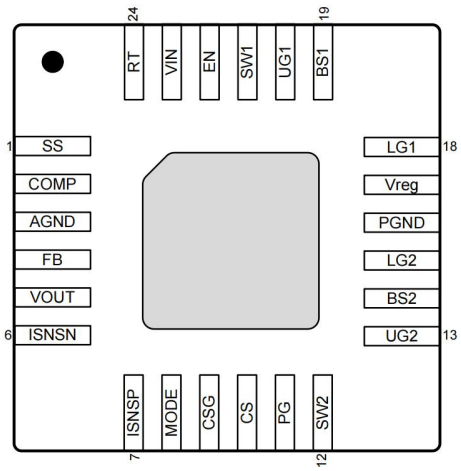
14. Place the Vreg bypass capacitor near the controller IC and connect it between the Vreg and PGND pins. Usually 2.2 μ F ceramic capacitors are used.

15. The exposed solder pads of the package should be soldered to a metal area of equivalent size on the PCB. This area should be connected to the GND plane and connected to the back and middle layers of the PCB through multiple vias. The GND plane area connected to the exposed solder pad should be maximized to improve thermal performance.

16. It is recommended to use multi-layer PCB design.

Pin Description

Top view



(QFN4x4-24)

PIN	NAME	FUNCTION
1	SS	Soft start programming pin. The capacitor between the SS pin and AGND pin is used to program the soft start time.
2	COMP	Compensation pin. This pin is used to compensate and adjust the control loop. Connect the serial RC network from the COMP pin to GND.
3	AGND	Simulate ground pin.
4	FB	Voltage feedback input pin. Connect FB and VOUT through a resistive voltage divider.
5	VOUT	Output voltage pin. Connect to the output capacitor.
6, 7	ISNSN, ISNSP	Output current detection amplifier input. The optional current detection resistor connected between ISNSN and ISNSP can be located on the output side of the converter.
8	MODE	Connect this pin to AGND using a 100kΩ resistor.
9	CSG	The negative input or ground input of the PWM current detection amplifier. Directly connected to the low end (ground) of the current detection resistor.
10	CS	Positive input of PWM current detection amplifier.
11	PG	The power supply indicates normal open leakage output. When the F-ultrasound shows a 0.8V ± 10% adjustment window, PGOOD is pulled down.
12, 21	SW2, SW1	The switch nodes are on the boost side and the buck side, respectively.
13, 20	UG2, UG1	Output of high-end gate driver. Directly connected to the gate of the high-end MOSFET.
14, 19	BS2, BS1	High end gate driven boost input. Suggest connecting a 100nF capacitor between this pin and SW1, SW2. It can enhance the gate drive to fully open the internal high-end NMOS.
15, 18	LG2, LG1	The output of the low side gate driver. Directly connected to the gate of the low side MOSFET.
16	PGND	The power ground of the IC. Connect to the high current ground of the low side gate driver.
17	Vreg	Output of VCC bias regulator. Ground the 2.2μF to 4.7μF capacitors.
22	EN	Enable input pins. This pin provides digital control to turn on or off the converter.
23	VIN	Power input pin.
24	RT	Switching frequency programming pin. External resistors are connected to the RT pin and AGND to set the switching frequency.
Power Pad	-	Bare solder pads. Connect to PCB ground.

Order Information

PN	Package	Package quantity
AD9575ET0	QFN4x4-24L	5000PCS

Absolute Maximum Ratings (1)

Input power supply voltage V_{IN} ..... -0.3V ~ 42V
Enable pin voltage V_{EN} ..... -0.3V ~ 42V
SW voltage V_{SW1}, V_{SW2} ..... -0.3V(-5V for < 10ns) ~ 42V (46V for < 5ns)
BS1 and UG1 voltage V_{BS1}, V_{UG1} relative to SW1 ..... -0.3 ~ (VSW + 6V)
BS2 and UG2 voltage V_{BS2}, V_{UG2} relative to SW2 ..... -0.3 ~ (VSW + 6V)
V_{OUT} , ISNSP, ISNSN voltage ..... -0.3V ~ 28V
Other pin voltages ..... -0.3V ~ 6V
Maximum junction temperature ..... 150°C
Storage temperature ..... -55°C ~ 150°C
Lead temperature (welding for 10 seconds) ..... 260°C
ESD Classification(HBM) ..... Class 2
Dissipative power(P_D) @ TA = 25°C 1.92W

Recommended working conditions (2)

Input power supply voltage V_{IN} ..... 5V ~ 40V
Environmental temperature T_A ..... -40°C ~ 85°C

Thermal properties

QFN4x4-24(Bare solder pads), θ_{JA} ..... 52°C/W
QFN4x4-24(Bare solder pads), θ_{JC} ..... 7°C/W

Note 1: Exceeding these rated values may damage the equipment.

Note 2: If it exceeds its working conditions, the normal operation of the equipment cannot be guaranteed.

Electrical Charcteristics

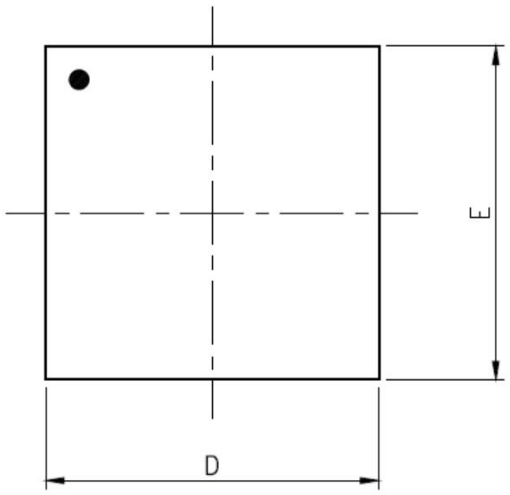
V_{IN}=12V, T_A=25°C,unlessotherwisespecified.

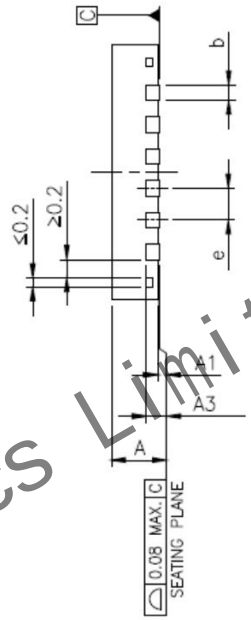
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage V_{IN}						
Input power supply voltage range			4.5		40	V
Static current (non switching)	I_Q	V_{FB} = 1V		2		mA
Standby power current (no load)				6		mA
Voltage regulator V_{reg}						
adjust voltage	V_{reg}			5.4		V
EA（Error Amplifier）						
Reference voltage	V_{REF}	9V≦V_{IN}≦40V		808		mV
Error amplifier transconductance	GM_{EA}			1.3		mS
COMP current injection/pulling	I_{sink}/I_{source}	V_{FB}= V_{REF}±0.3V		250		uA
Frequency						
Switching frequency	F_{SW}	RT=100KΩ		260		KHz
Limit threshold						
Buck current limiting threshold	$V_{CS(BUCK)}$			76		mV
Boost current limit threshold	$V_{CS(BOOST)}$			170		mV
Constant current loop						
Reference voltage for regulating average current loop	V_{SNS}			50		mV
Power supply normal indication pin trip threshold range						
FB Trip Threshold Reduction		Respect to V_{REF}		-10		%
FB rising trip threshold		Respect to V_{REF}		10		%
Enable/Under-voltage Lockout						
EN High-level input voltage	V_{ENH}		1.8			V
EN Low-Level Input Voltage	V_{ENL}				0.4	V
Input UVLO threshold		VIN Rising		4.2	4.5	V
Undervoltage lockout threshold hysteresis voltage				650		mV
Soft start						
Soft-start pull-up current	I_{SS}	V_{SS} = 0		6		uA
Soft start clamping voltage	$V_{SS(CLP)}$	SS Open		1.46		V
Soft start clamping voltage						
Hot shutdown threshol(3)				160		℃

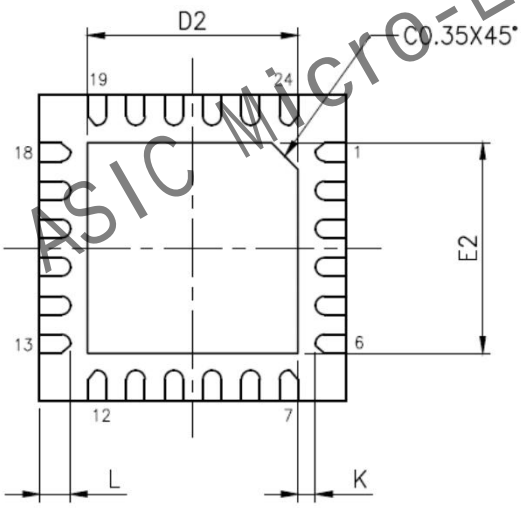
Note 3: Guaranteed by design.

Package Description

QFN4X4-24L Dimensions







UNIT:mm

SYMBOLS	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
K	0.20	---	---
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45