

2-Lines, Bi-directional, Transient Voltage Suppressors

Features

- ◆ Stand-off voltage: $\pm 5V$ Max.
- ◆ Transient protection for each line according to
IEC61000-4-2(ESD): $\pm 30kV$ (contact)
IEC61000-4-4 (EFT): 40A (5/50ns)
IEC61000-4-5(surge): 7A (8/20 μs)
- ◆ Ultra-low capacitance: $C_J = 17pF$ typ.
- ◆ Low leakage current:
- ◆ Low clamping voltage: $V_{CL} = 9.3V$ typ. @ $I_{PP} = 16A$ (TLP)
- ◆ Solid-state silicon technology

Applications

- ◆ Cellular handsets
- ◆ Tablets
- ◆ Laptops
- ◆ Other portable devices
- ◆ Network communication devices

Descriptions

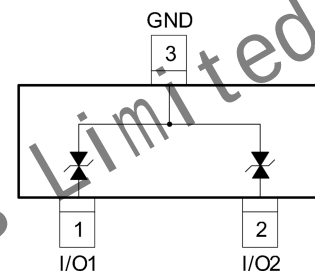
AE0512PKL0 is a bi-directional TVS (Transient Voltage Suppressor). It has been specifically designed to protect sensitive electronic components which are connected to low speed data lines and control lines from over-stress caused by ESD (Electrostatic Discharge), EFT (Electrical Fast Transients) and Lightning.

AE0512PKL0 may be used to provide ESD protection up to $\pm 30KV$ (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 7A (8/20 μs) according to IEC61000-4-5.

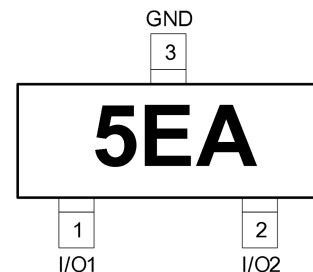
AE0512PKL0 is available in SOT-523 package. Standard products are Pb-free and Halogen-free.



SOT-523 (Bottom View)



Pin configuration



5EA= Device code

Marking (Top View)

Order information

Device	Package	Shipping
AE0512PKL0	SOT-523	3000/Tape & Reel

Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	77	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{PP}	7	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 30	kV
ESD according to IEC61000-4-2 contact discharge		± 30	
Junction temperature	T_J	125	$^{\circ}C$
Operating temperature	T_{OP}	-40~85	$^{\circ}C$
Lead temperature	T_L	260	$^{\circ}C$
Storage temperature	T_{STG}	-55~150	$^{\circ}C$

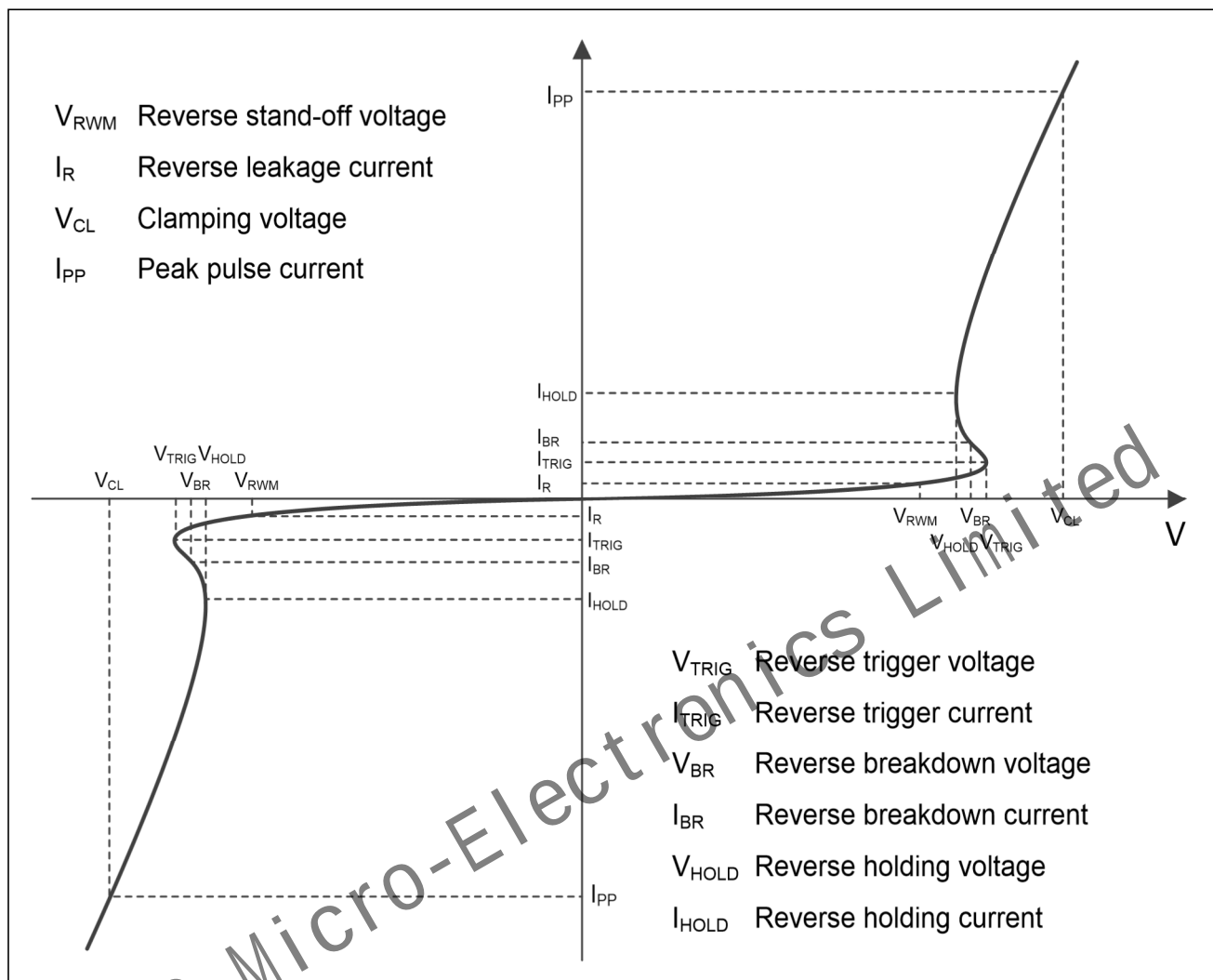
Electrical characteristics ($T_A = 25^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	V_{RWM}				± 5.0	V
Reverse leakage current	I_R	$V_{RWM} = 5.0V$			100	nA
Reverse breakdown voltage	V_{BR}	$I_{BR} = 1mA$	5.5	6.5		V
Reverse holding voltage	V_{HOLD}	$I_{HOLD} = 50mA$	5.5	6.5		V
Clamping voltage ¹⁾	V_{CL}	$I_{PP} = 16A, t_p = 100ns$		10.0		V
Dynamic resistance ¹⁾	R_{DYN}			0.2		Ω
Clamping voltage ²⁾	V_{CL}	$V_{ESD} = 8kV$		10.0		V
Clamping voltage ³⁾	V_{CL}	$I_{PP} = 1A, t_p = 8/20\mu s$		6.2	7	V
		$I_{PP} = 7A, t_p = 8/20\mu s$		9.3	11	V
Junction capacitance	C_J	$V_R = 0V, f = 1MHz$		17	20	pF
	C_J	$V_R = 2.5V, f = 1MHz$		15	18	pF

Notes:

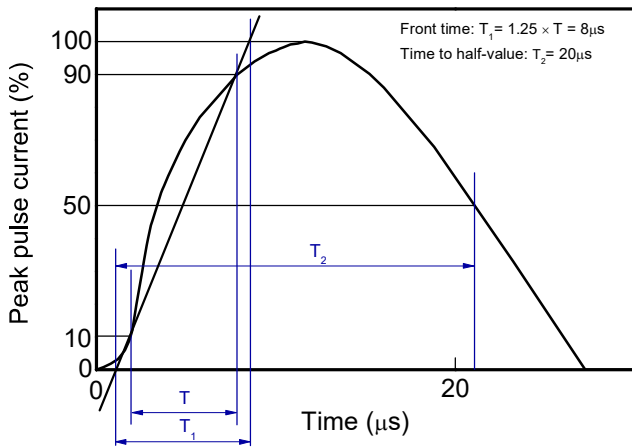
- 1) TLP parameter: $Z_0 = 50\Omega$, $t_p = 100ns$, $t_r = 2ns$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
- 2) Contact discharge mode, according to IEC61000-4-2.
- 3) Non-repetitive current pulse, according to IEC61000-4-5.

Electrical characteristics ($T_A=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

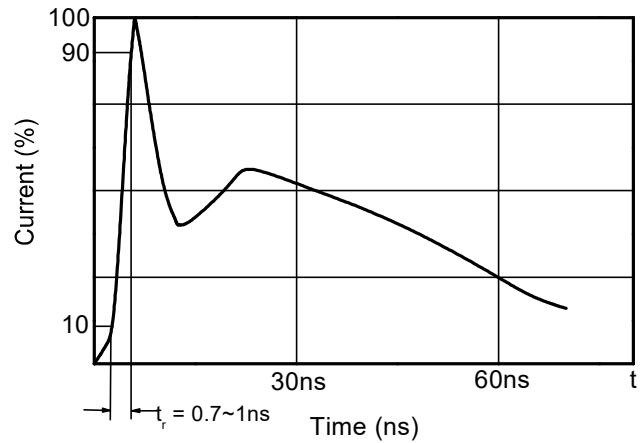


Definitions of electrical characteristics

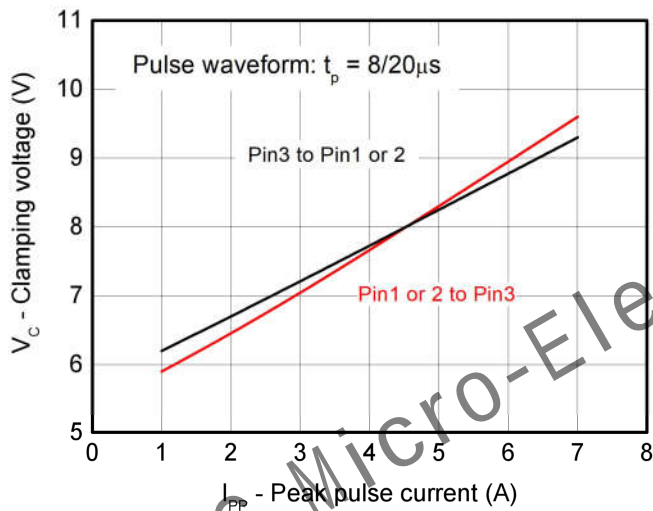
Typical characteristics (TA = 25 °C, unless otherwise noted)



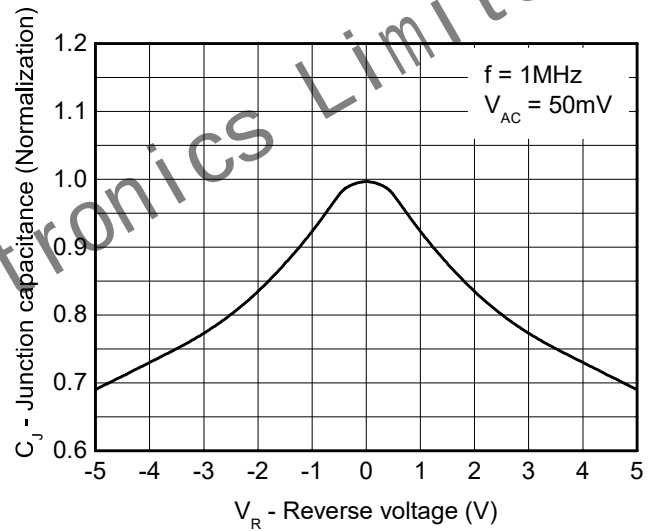
8/20μs waveform per IEC61000-4-5



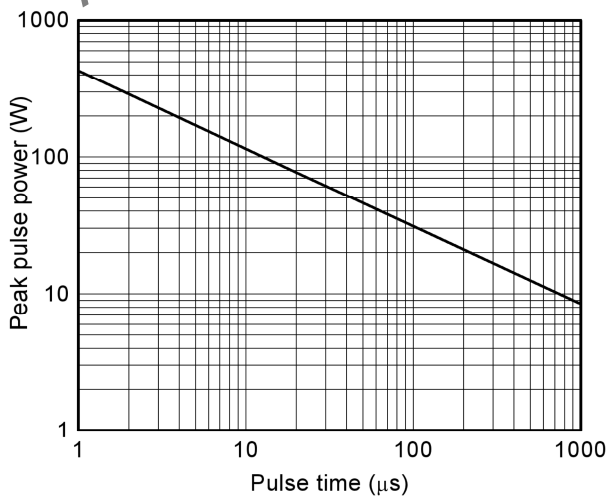
Contact discharge current waveform per IEC61000-4-2



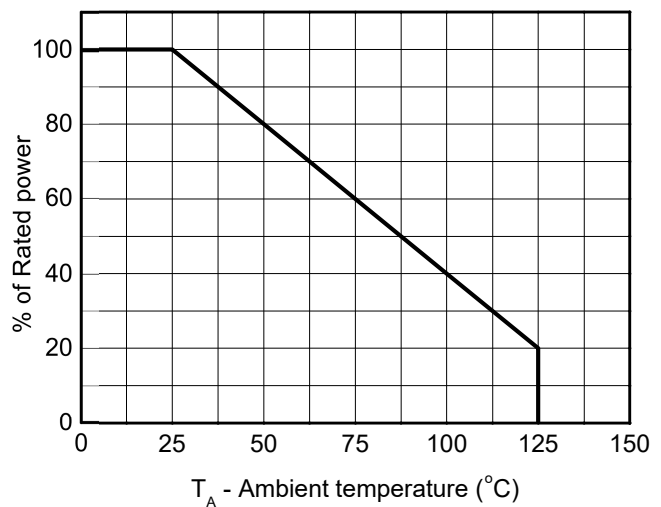
Clamping voltage vs. Peak pulse current



Capacitance vs. Reverse voltage

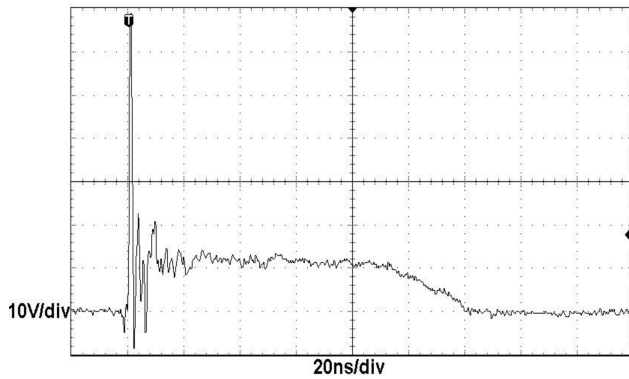


Non-repetitive peak pulse power vs. Pulse time

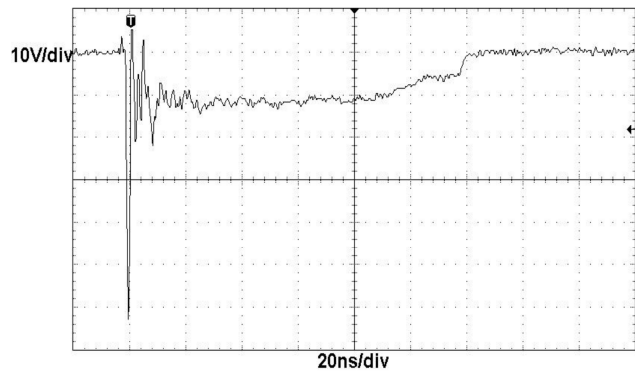


Power derating vs. Ambient temperature

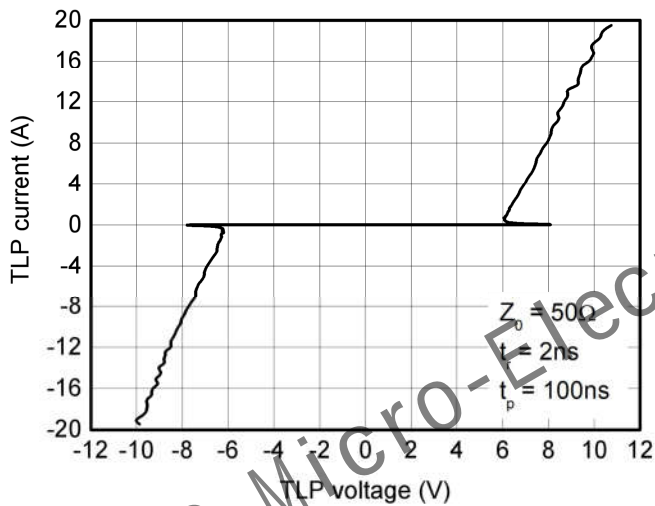
Typical characteristics (TA = 25 °C, unless otherwise noted)



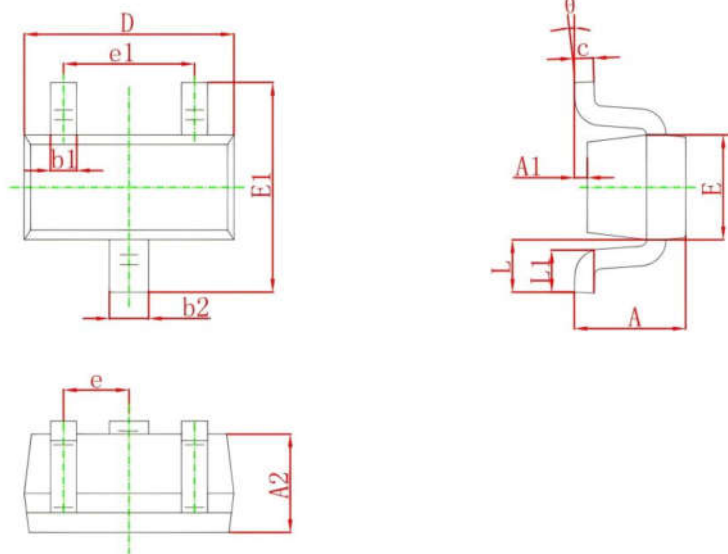
ESD clamping
(+8kV contact discharge per IEC61000-4-2)



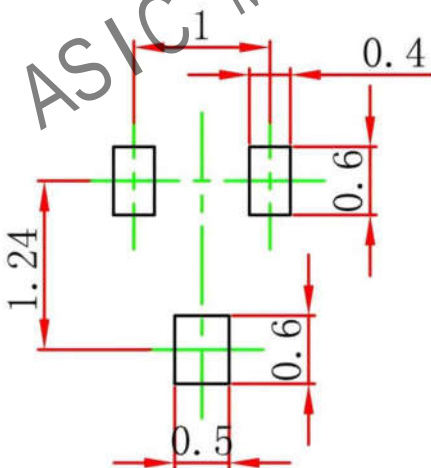
ESD clamping
(-8kV contact discharge per IEC61000-4-2)



TLP Measurement

PACKAGE OUTLINE DIMENSIONS
SOT-523


Symbol	Dimensions in millimeters		
	Min.	Typ.	Max.
A	0.680	-	0.900
A1	0.000	-	0.100
A2	0.630	-	0.830
b1	0.150	-	0.250
b2	0.250		0.350
c	0.050	-	0.200
D	1.480	-	1.700
E	0.700	-	0.900
E1	1.450	-	1.850
e	0.500TYP		
e1	0.900	-	1.100
L	0.400REF		
L1	0.200	-	0.500
θ	0°	-	8°

Recommend land pattern (Unit: mm)

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.